REMARKS

Claims 1-3, 5-13, and 15-36 were pending in the application. Claims 2, 8, 12, 20, 28 and 35 have been cancelled. Claims 1, 7, 11, 19, 25 and 30 have been amended. Applicant submits that the amendments do not raise any new issues of patentability, and thus respectfully requests their entry into the record. Claims 1, 3, 5-7, 9-11, 13, 15-19, 21-27, 29-34 and 36 remain pending in the application.

35 U.S.C. § 103 Rejections:

Claims 1-3, 7-9, 11-13, and 19-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Motika, U.S. Patent 5,982,189, in view of Kohno, U.S. Patent 5,943,285. Claims 25, 29, 30 and 36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kraus, U.S. Patent 6,587,979, in view of Kohno. Claims 5, 15, 18 and 24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Motika in view of Kohno and in further view of Au, U.S. Patent 6,681,359. Claims 6, 10, 16, and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Motika in view of Kohno, Zuraski, U.S. Patent 6,560,740, and in further view of Lo, U.S. Patent 5,661,732. Claims 26, 27, 31 and 32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kraus in view of Kohno and in further view of Lo. Claims 28 and 33 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kraus in view of Kohno and in further view of Motika. Claim 34 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Kraus in view of Kohno and Au. Claim 35 was rejected under 35 U.S.C. § 103(a) over Kraus in view Kohno and in view of Arimilli, U.S. Patent 6,665,828. With regard to those claims that have been cancelled, Applicant believes these rejections to now be moot. With respect to the remaining claims, Applicant respectfully traverses these rejections.

The prior art does not suggest the desirability of the claimed invention. The teachings of Motika were presented in the previous office action response. Kohno teaches a semiconductor memory device adapted to enhance functional features and a large memory capacity. The semiconductor memory device includes a semiconductor

chip divided into 9 regions having an identical area, in a 3.times.3 pattern. A main control block is arranged at least in a central region and memory blocks are arranged respectively in the peripheral regions. Each of the memory blocks is controlled by the main control block and includes a data input/output circuit and a memory control circuit.

Kraus teaches a flexible built-in self-test (BIST) circuit incorporated into an integrated circuit (IC) for testing one or random access memories or other memories embedded in an integrated circuit regardless of the number, size or test requirements of the memories. Input data from a controller that may be conveniently partitioned among components internal and external to the IC, supplies data to the BIST circuit indicating the size of the embedded memories to be tested and selecting from among several modes of BIST operation.

In contrast, Independent claim 1 recites, in pertinent part:

> "A built-in self-test controller, comprising: ...a memory built-in self-test engine operating a predetermined one of the memory built-in self-test state machines; and a logic built-in self-test engine; wherein the built-in self-test controller is geographically centralized within an integrated circuit" (Emphasis added).

Independent claims 7, 11, 19, 25 and 30 recite similar combinations of features.

Applicant submits that the prior art combination of Motika and Kohno does not suggest the desirability of the combinations recited in independent claims 1, 7, 11 and 19. In particular, Kohno does not provide any teaching or suggestion of placing a built-in self-test controller including a logic built-in self-test engine in a geographically centralized location within an integrated circuit. In the Office Action, the Examiner states that it would be obvious to apply the centralized them of Kohno to the controller taught by Au and Motika in order to produce a better self-testing product. However, Applicant notes that Kohno is directed to a semiconductor memory device. Thus, Applicant submits that Kohno does not provide any suggestion to modify Motika in order

to include a built-in self-test controller including a **logic** built-in self-test engine in a location that is geographically centralized within an integrated circuit.

Applicant further submits that the prior art combination of Kraus and Kohno does not suggest the desirability of the combinations recited in claims 25 and 30. Kraus, as noted above, is directed to the testing of memories. Kohno, as also noted above, is directed towards a semiconductor memory device. Thus, Applicant submits that Kohno does not provide any suggestion to modify Kraus in order to obtain a built-in self-test controller, including a **logic** built-in self-test engine, in a geographically centralized location.

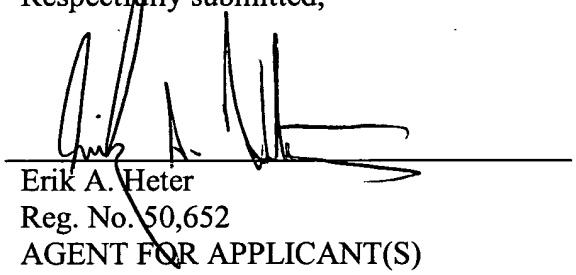
Thus, for at least the reasons stated above, Applicant submits that the cited references do not teach or suggest the desirability of the combinations of features recited in the independent claims. Accordingly, removal of the 35 U.S.C. § 103(a) rejections of the independent claims, as well as those rejections directed to various ones of the associated dependent claims, is respectfully requested.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-56100/BNK.

Respectfully submitted,



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